AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-30. (Cancelled).

31. (Previously Presented) A method of assigning thread priority comprising:

assigning priority to a first thread in a multi threaded processor; and

assigning priority to a second thread in response to one of a plurality of conditions being true, the conditions consisting of

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread, and wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

32. (Previously Presented) A processor, comprising:

control logic to assign priority to one of at least first and second threads; and a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread, and to increment a value stored in said first starting counter if there is an indication of approaching instruction side starvation for said first thread,

and wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

33. (Previously Presented) The processor of claim 32 wherein said control logic is to increment the value stored in the first starting counter geometrically.

34. (Previously Presented) The processor of claim 33 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

35. (Previously Presented) A processor comprising:

control logic to assign priority to a first thread and to assign priority to a second thread in response to one of a plurality of conditions being true, the conditions consisting of

if a processing counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread

wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

36. (New) A computer system comprising:

a memory to store instructions for first and second threads;

a processor including

control logic coupled to said memory to assign priority between said first and second threads; and

a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread and to increment a value stored in said first starting counter in response to an indication of approaching instruction side starvation for said first thread,

wherein a preliminary value for said thread precedence counter is based on a value stored in a first starting counter associated with said first thread, and

wherein said control logic is determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

37. (New) The computer system of claim 36 wherein said control logic is to increment the value stored in the first starting counter geometrically.

38. (New) The computer system of claim 37 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

39. (New) A computer system comprising:

a memory to store instructions for first and second threads;

a processor including

control logic to assign priority to said first thread and to assign priority to said second thread in response to one of a plurality of conditions being true, the conditions consisting of:

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and if there is not an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread,

wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

40. (New) A set of instructions residing in a storage medium, said set of instructions to be executed by a processor to handle processing of at least first and second threads in parallel and assign thread priority comprising:

assigning priority to said first thread;

loading a preliminary value to a thread precedence counter;

assigning priority to said second thread after said thread precedence counter expires;

determining if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread; and

incrementing a value stored in said first starting counter is incremented in response to an indication of approaching instruction side starvation for said first thread,

wherein said preliminary value is based on a value stored in a first starting counter associated with said first thread, and

wherein determining if there is an indication of approaching instruction side starvation for said first thread includes determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

41. (New) The set of instructions of claim 40 wherein said value is incremented geometrically.

42. (New) The set of instructions of claim 41 wherein said value is incremented geometrically by left-shifting a binary 1 bit into said value.